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Cai

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(54) **PIXEL DRIVING CIRCUIT AND OLED DISPLAY DEVICE THAT EFFECTIVELY COMPENSATE FOR THRESHOLD VOLTAGE IMPOSED ON A DRIVING TFT**

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H01L 27/32	(2006.01)
H01L 51/52	(2006.01)
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G09G 3/3233	(2016.01)

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See application file for complete search history.

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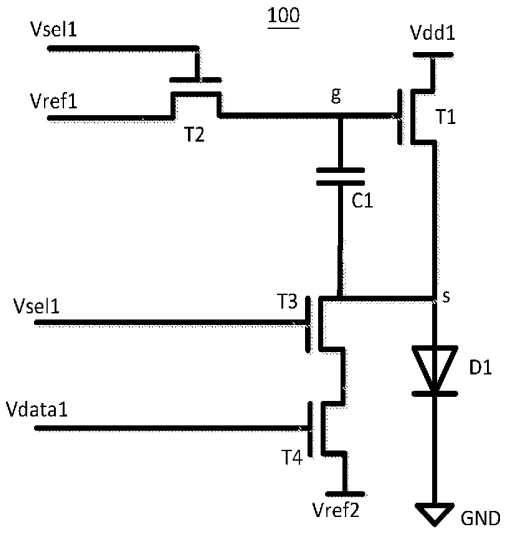
(57) **ABSTRACT**

A pixel driving circuit and an OLED display are provided. The pixel driving circuit includes a first TFT, a second TFT, a third TFT, a fourth TFT, a capacitor, and an OLED. A gate of the third TFT is coupled to the scanning signal. A source of the third TFT is coupled to a drain of the fourth TFT. A gate of the fourth TFT is coupled to a data signal and a source of the fourth is coupled to a second reference voltage signal. The fourth TFT controls the electric current of the first TFT with the data signal and the second reference signal during the compensation stage of threshold voltage. Further, the compensation voltage of the first TFT is compensated.

11 Claims, 7 Drawing Sheets



(52) **U.S. Cl.**
CPC *G09G 2310/0262* (2013.01); *G09G 2310/0264* (2013.01); *G09G 2320/043* (2013.01)

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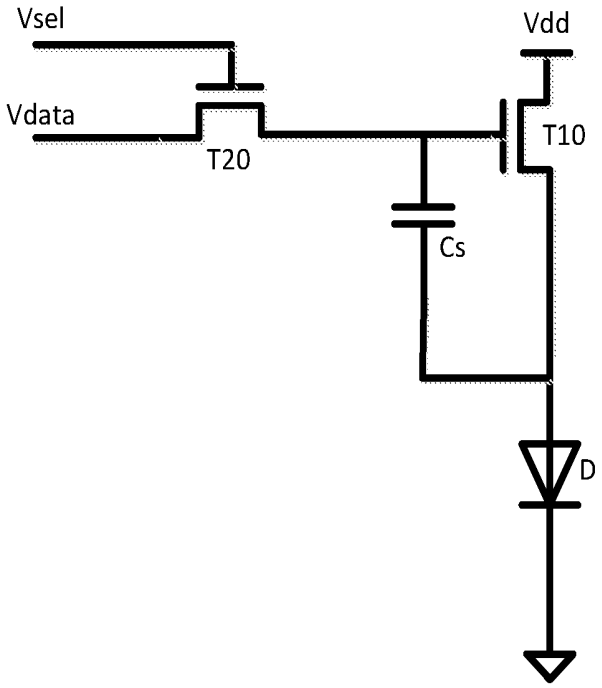


Fig. 1 (Related art)

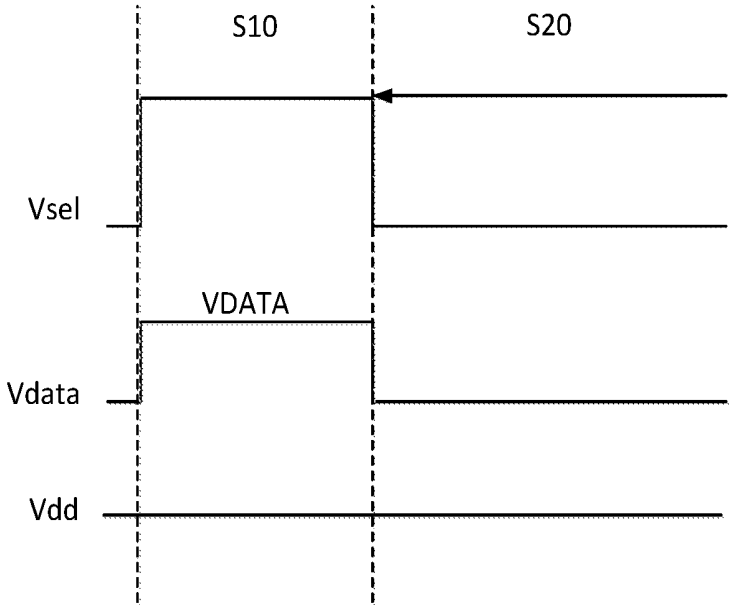
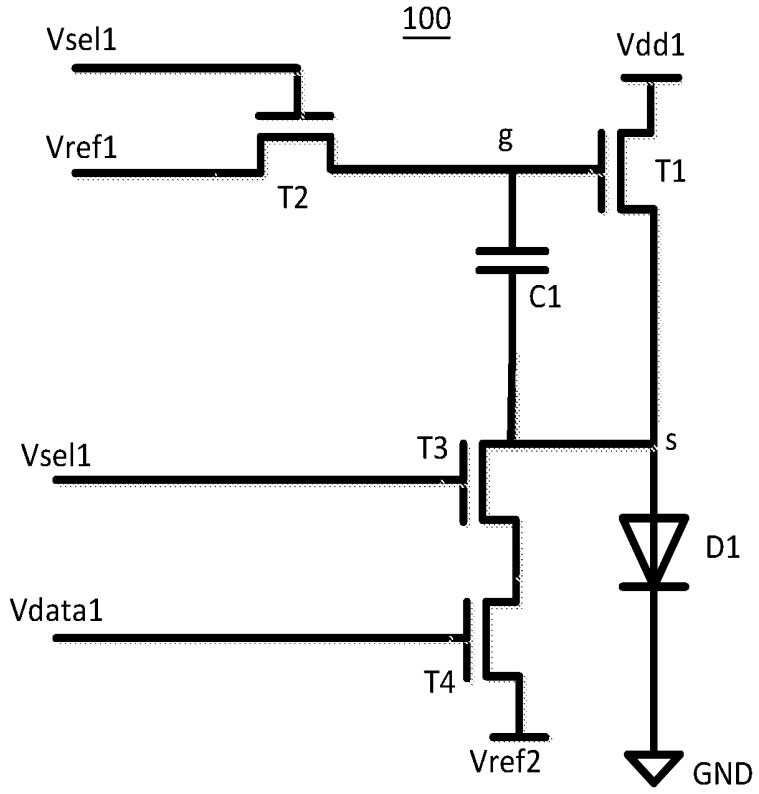


Fig. 2 (Related art)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Vsel1
Vdd1
Vref1
g
T1
T2
C1
Vsel1
T3
s
D1
Vdata1
T4
Vref2
GND

Fig. 3

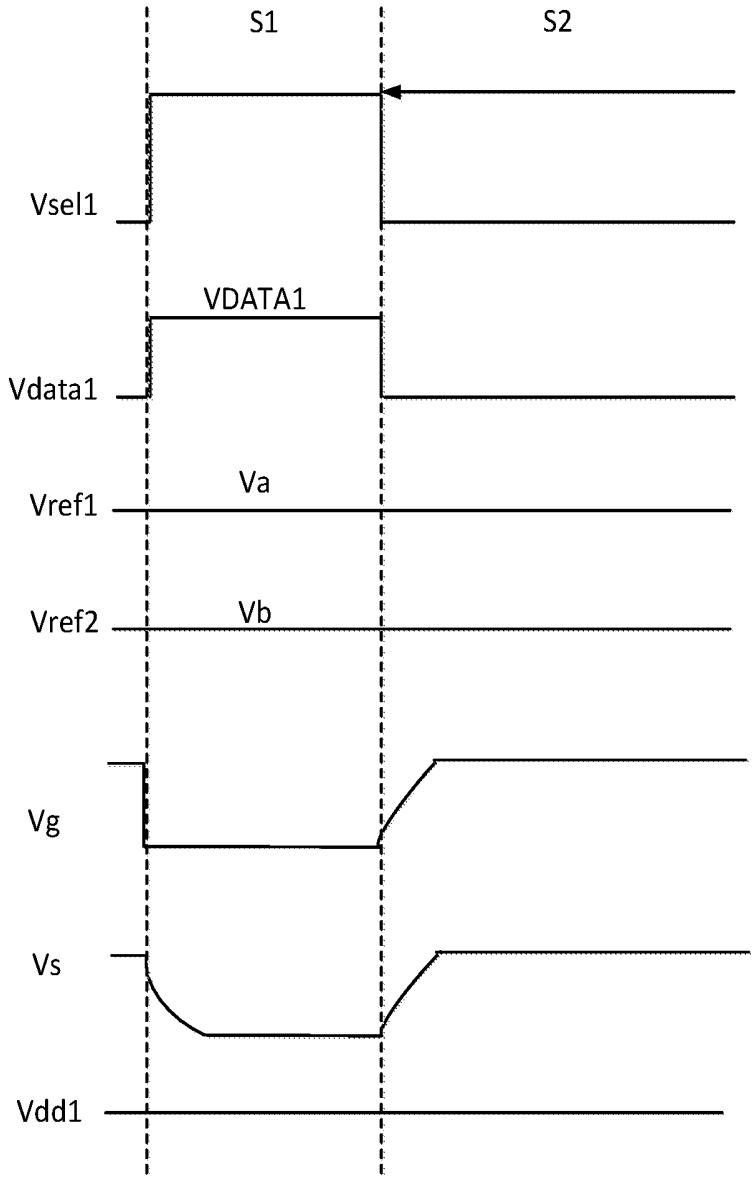


Fig. 4

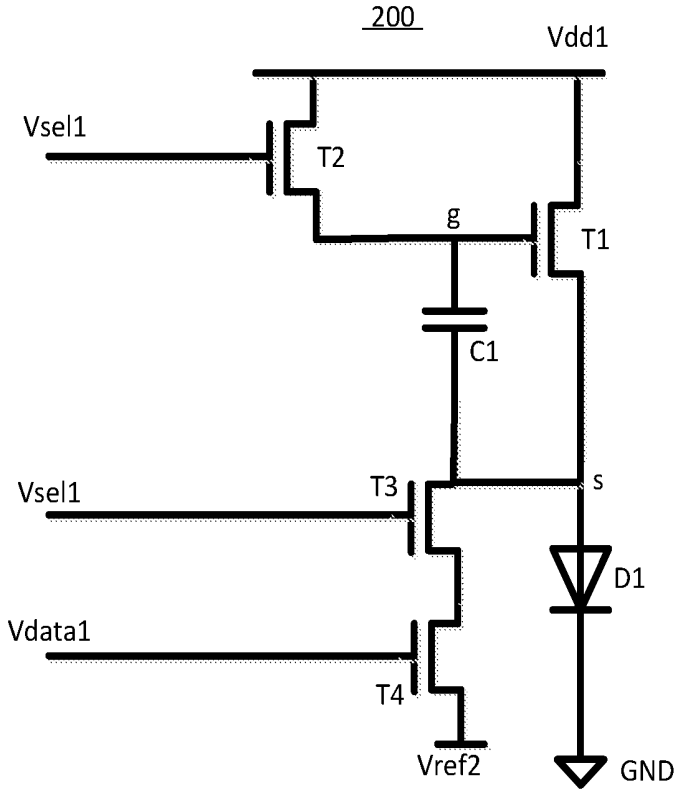


Fig. 5

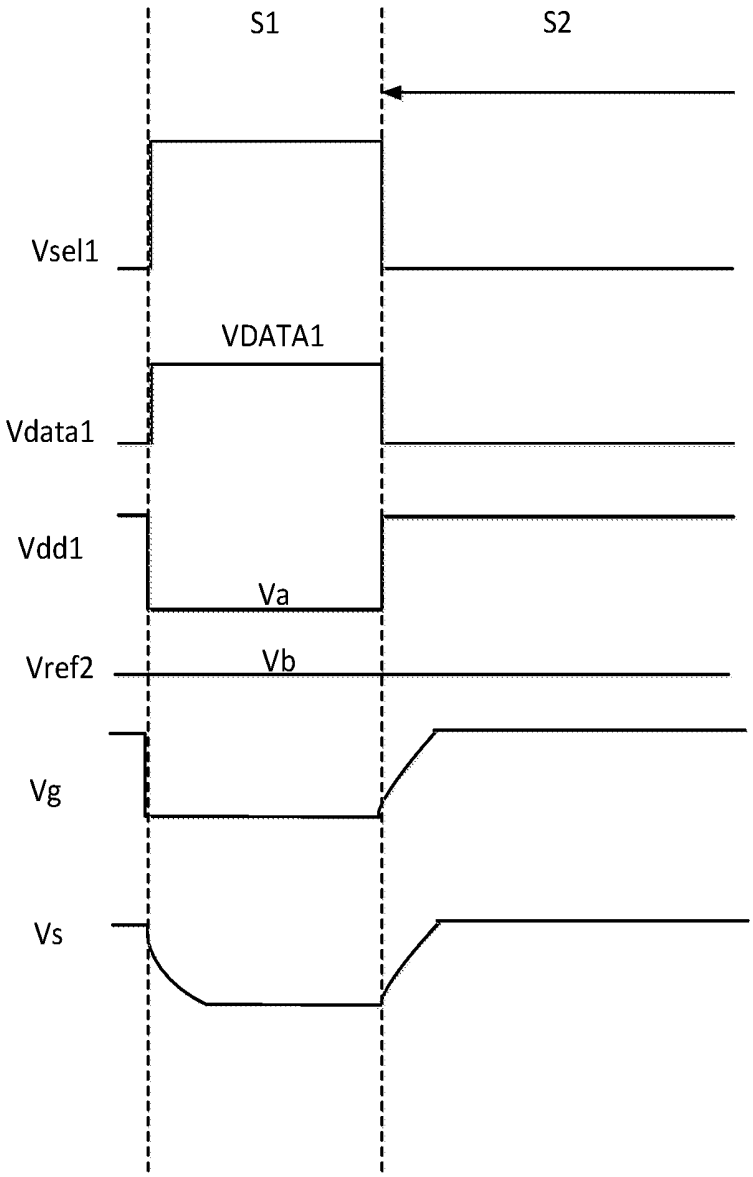
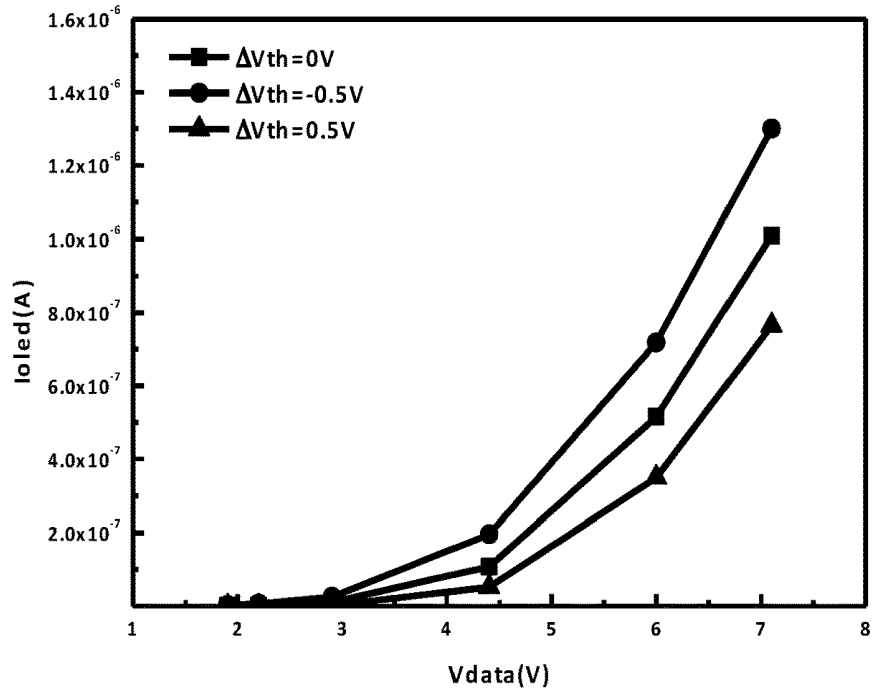


Fig. 6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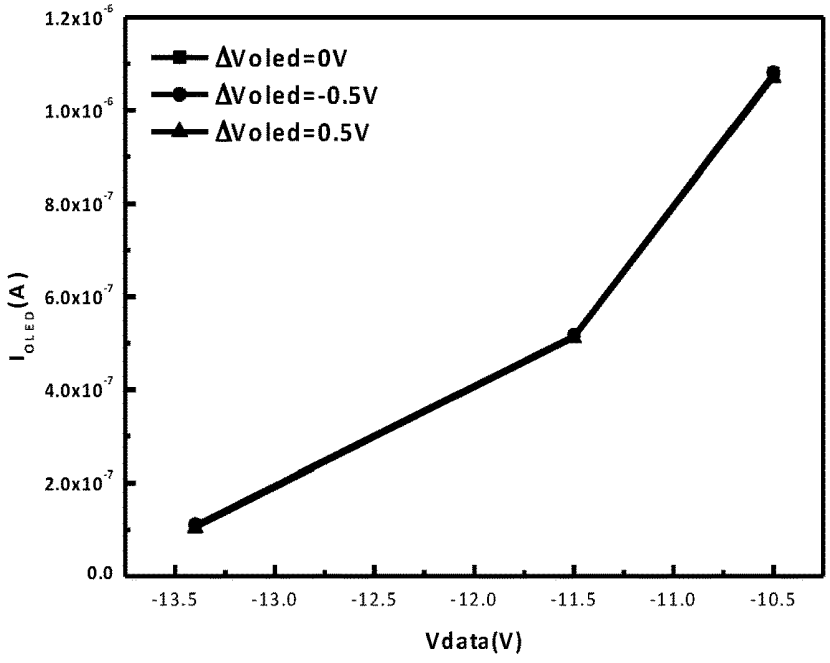
ΔVth=-0.5V
ΔVth=0.5V
Ioled(A)
Vdata(V)

Fig. 7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ΔVoled=-0.5V
ΔVoled=0.5V
I_OLED(A)
Vdata(V)

Fig. 8

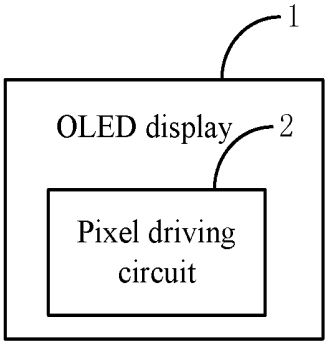

Fig. 9

PIXEL DRIVING CIRCUIT AND OLED DISPLAY DEVICE THAT EFFECTIVELY COMPENSATE FOR THRESHOLD VOLTAGE IMPOSED ON A DRIVING TFT

BACKGROUND

1. Field of the Disclosure

The present disclosure relates to the field of liquid crystal display, and more particularly, to a pixel driving circuit and an organic light-emitting diode (OLED) display device.

2. Description of Related Art

An OLED display device of related art is recognized by the industry to have an extremely developmental potential because the OLED display device has advantages of compactness, simple structure, self-illumination, high brightness, wide viewing angle, short response time, etc.

The OLED device is an electric current driven device. The electric current flows through the OLED to make the OLED give out light. The brightness of the OLED is determined by the electric current. Most integrated circuits (ICs) of related art merely transmits voltage signals so the pixel driving circuit of the OLED needs to transforming a voltage signal into an electric current signal. The pixel driving circuit of related art is a 2T1C pixel with the structure of two TFTs and one capacitor. With the structure, the pixel driving circuit can transform the voltage into the electric current. However, the pixel driving circuit of related art does not have the function of compensation.

FIG. **1** is a circuit diagram of a 2T1C pixel driving circuit of related art. The 2T1C pixel driving circuit includes a first thin-film transistor (TFT) T**10**, a second TFT T**20**, and a capacitor Cs. The first TFT T**10** is a driving TFT. The second TFT T**20** is a switch TFT. The capacitor Cs is a storage capacitor. Specifically, agate of the second TFT T**20** is electrically connected to a scanning signal Vsel. A source of the second TFT T**20** is electrically connected to a data signal Vdata. A drain of the second TFT T**20** is electrically connected to agate of the first TFT T**10**. A drain of the first TFT T**10** is electrically connected to a power signal Vdd. A source of the first TFT T**10** is electrically connected to an anode node level of the OLED D. A cathode of the OLED D is electrically connected to a ground terminal. One terminal of the capacitor Cs is electrically connected to a drain of the second TFT T**20**. The other terminal of the capacitor Cs is electrically connected to the source of the first TFT T**10**.

Please refer to FIG. **2** as well. FIG. **2** illustrates a timing diagram of a 2T1C pixel driving circuit as illustrated in FIG. **1**. The working process of the 2T1C pixel driving circuit is divided into a first working stage S**10** and a second working stage S**20**. At the first working stage S**10**, the data signal Vdata is a display data signal VDATA, and the scanning signal Vsel is at high voltage level. At the first working stage S**20**, the data signal Vdata is at low voltage level, and the scanning signal Vsel is at low voltage level as well. At the first working stage S**10** and the second working stage S**20**, the power signal Vdd is constant high voltage.

In the present embodiment, the OLED D gives out light at the second working stage S**20**. Meanwhile, a gate-source voltage V_{gs} imposed on the first TFT T**10**, which drives the OLED D to light, satisfies the following equation:

$$V_{gs}=VDATA-V_{OLED};$$

where VDATA indicates the data signal at high voltage level, and V_{OLED} indicates voltage level of an anode node of the OLED D.

As the equation tells, the gate-source voltage V_{gs} for driving illumination of the OLED D is irrelevant to the threshold voltage imposed on the first TFT T**10**. Therefore, the 2T1C pixel driving circuit fails to compensate the threshold voltage imposed on the driving TFT, i.e., the first TFT T**10**.

SUMMARY

An object of the present disclosure is to propose a pixel driving circuit and an organic light-emitting diode (OLED) display device to effectively compensate for threshold voltage imposed on a driving TFT because of change.

According to a first aspect of the present disclosure, a pixel driving circuit includes a first thin-film transistor (TFT), a second TFT, a third TFT, a fourth TFT, a capacitor, and an organic light-emitting diode (OLED). A gate of the first TFT is electrically connected to a first node, a source of the first TFT electrically connected to a second node, and a drain of the first TFT electrically connected to a power signal. A gate of the second TFT is electrically connected to a scanning signal, a source of the second TFT is electrically connected to a first reference voltage signal, and a drain of the second TFT is electrically connected to the first node. A gate of the third TFT is electrically connected to the scanning signal. A source of the third TFT is electrically connected to a drain of the fourth TFT. A drain of the third TFT is electrically connected to the second node. A gate of the fourth TFT is electrically connected to a data signal, and a source of the fourth is electrically connected to a second reference voltage signal. One terminal of the capacitor is electrically connected to the first node. The other terminal of the capacitor is electrically connected to the second node. An anode of the OLED is electrically connected to the second node. A cathode of the OLED is electrically connected to a ground terminal. The first reference voltage signal is the power signal. A voltage across a gate and a source of the first TFT satisfies the following equation:

$$V_{gs}=\left[\left(\frac{W}{L}\right)_{T4}/\left(\frac{W}{L}\right)_{T1}\right]^{\frac{1}{2}}(VDATA1-Vb-Vth3)+Vth1;$$

where Vgs indicates the voltage across a gate and a source of the first TFT; Vb indicates a second reference voltage provided by the second reference voltage signal;

$$\left(\frac{W}{L}\right)_{T4}$$

indicates the ratio of the width to the length of a channel of the fourth TFT;

$$\left(\frac{W}{L}\right)_{T1}$$

indicates the ratio of the width to the length of a channel of the first TFT; VDATA**1** is a display data signal at high voltage level provided by the data signal; Vth**3** is a threshold voltage imposed on the third TFT; Vth**1** is the threshold voltage imposed on the first TFT.

According to a second aspect of the present disclosure, a pixel driving circuit includes a first thin-film transistor

(TFT), a second TFT, a third TFT, a fourth TFT, a capacitor, and an organic light-emitting diode (OLED). A gate of the first TFT is electrically connected to a first node, a source of the first TFT electrically connected to a second node, and a drain of the first TFT electrically connected to a power signal. A gate of the second TFT is electrically connected to a scanning signal, a source of the second TFT is electrically connected to a first reference voltage signal, and a drain of the second TFT is electrically connected to the first node. A gate of the third TFT is electrically connected to the scanning signal. A source of the third TFT is electrically connected to a drain of the fourth TFT. A drain of the third TFT is electrically connected to the second node. A gate of the fourth TFT is electrically connected to a data signal, and a source of the fourth is electrically connected to a second reference voltage signal. One terminal of the capacitor is electrically connected to the first node. The other terminal of the capacitor is electrically connected to the second node. An anode of the OLED is electrically connected to the second node. A cathode of the OLED is electrically connected to a ground terminal.

According to a third aspect of the present disclosure, an organic light-emitting diode (OLED) display includes a pixel driving circuit. The pixel driving circuit includes a first thin-film transistor (TFT), a second TFT, a third TFT, a fourth TFT, a capacitor, and an organic light-emitting diode (OLED). A gate of the first TFT is electrically connected to a first node, a source of the first TFT electrically connected to a second node, and a drain of the first TFT electrically connected to a power signal. A gate of the second TFT is electrically connected to a scanning signal, a source of the second TFT is electrically connected to a first reference voltage signal, and a drain of the second TFT is electrically connected to the first node. A gate of the third TFT is electrically connected to the scanning signal. A source of the third TFT is electrically connected to a drain of the fourth TFT. A drain of the third TFT is electrically connected to the second node. A gate of the fourth TFT is electrically connected to a data signal, and a source of the fourth is electrically connected to a second reference voltage signal. One terminal of the capacitor is electrically connected to the first node. The other terminal of the capacitor is electrically connected to the second node. An anode of the OLED is electrically connected to the second node. A cathode of the OLED is electrically connected to a ground terminal.

The present disclosure can bring beneficiary effects as describes: The fourth TFT is introduced in pixel driving circuit and the OLED display device to control the electric current of the first TFT with the data signal and the second reference signal during the compensation stage of threshold voltage. Further, the compensation voltage of the first TFT (i.e., a driving TFT) is compensated. Because of the introduction of the third TFT, the voltage level of a gate of the first TFT prevents from being affected by the second reference voltage sign during the lighting stage.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. **1** is a circuit diagram of a conventional 2T1C pixel driving circuit.

FIG. **2** illustrates a timing diagram of a 2T1C pixel driving circuit as illustrated in FIG. **1**.

FIG. **3** is a circuit diagram of a pixel driving circuit according to a first embodiment of the present disclosure.

FIG. **4** illustrates a timing diagram of the pixel driving circuit as illustrated in FIG. **3**.

FIG. **5** is a circuit diagram of a pixel driving circuit according to a second embodiment of the present disclosure.

FIG. **6** illustrates a timing diagram of a pixel driving circuit as illustrated in FIG. **5**.

FIG. **7** illustrates a relationship of the electric current flowing through the OLED when a drift value of the threshold voltage of the conventional 2T1C driving TFT and a drift value of the threshold voltage of the first TFT.

FIG. **8** illustrates a relationship of the electric current flowing through the OLED when a drift value of the threshold voltage of the driving TFT in the present disclosure and a drift value of the threshold voltage of the first TFT.

FIG. **9** is a schematic diagram of an organic light-emitting diode (OLED) display according to an embodiment of the present disclosure.

DETAILED DESCRIPTION OF THE EMBODIMENTS

The invention is described below in detail with reference to the accompanying drawings, wherein like reference numerals are used to identify like elements illustrated in one or more of the figures thereof, and in which exemplary embodiments of the invention are shown. This invention may, however, be embodied in many different forms and should not be construed as limited to the particular embodiments set forth herein. Rather, these embodiments are provided so that this disclosure will be thorough and complete, and will fully convey the scope of the invention to those skilled in the art. The drawings illustrate embodiments of the invention and, together with the description, serve to explain the principles of the invention.

FIG. **3** is a circuit diagram of a pixel driving circuit according to a first embodiment of the present disclosure. The pixel driving circuit **100** includes a first thin-film transistor (TFT) T**1**, a second TFT T**2**, a third TFT T**3**, a fourth TFT T**4**, a capacitor C**1**, and an organic light-emitting diode (OLED) D**1**. The first TFT T**1** is a driving TFT. The second TFT T**2** and the third TFT T**3** both are switch TFTs. The capacitor C**1** is a storage capacitor.

A gate of the first TFT T**1** is electrically connected to the first node g. A source of the first TFT T**1** is electrically connected to the second node s. A drain of the first TFT T**1** is electrically connected to a power signal Vdd**1**. A gate of the second TFT T**2** is electrically connected to a scanning signal Vsel**1**. A source of the second TFT T**2** is electrically connected to a first reference voltage signal Vref**1**. A drain of the second TFT T**2** is electrically connected to the first node g. A gate of the third TFT T**3** is electrically connected to the scanning signal Vsel**1**. A source of the third TFT T**3** is electrically connected to a drain of the fourth TFT T**4**. A drain of the third TFT T**3** is electrically connected to the second node s. A gate of the fourth TFT T**4** is electrically connected to the data signal Vdata**1**. A source of the fourth TFT T**4** is electrically connected to a second reference voltage signal Vref**2**. One terminal of the capacitor C**1** is electrically connected to the first node g. The other terminal of the capacitor C**1** is electrically connected to the second node s. An anode of the OLED D**1** is electrically connected to the second node s. A cathode of the OLED D**1** is electrically connected to a ground terminal GND.

In another embodiment, a thin-film transistor (TFT) T**1**, a second TFT T**2**, a third TFT T**3**, and a fourth TFT T**4** all are low temperature poly-silicon (LTPS) TFTs, oxide semiconductor TFTs, or amorphous silicon (α-Si) TFTs.

FIG. **4** illustrates a timing diagram of the pixel driving circuit **100** as illustrated in FIG. **3**. As FIG. **4** illustrates, the

working process of the pixel driving circuit **100** are divided into a compensation stage of threshold voltage Si and a lighting stage S**2**.

The first reference voltage signal Vref**1** and the second reference voltage signal Vref**2** both are constant low voltage in the working process of the pixel driving circuit **100**. The first reference voltage signal Vref**1** is configured to provide a first reference voltage Va. The second reference voltage signal Vref**2** is configured to provide a second reference voltage Vb. A power signal Vdd**1** is constant high voltage. The data signal Vdata**1** and the scanning signal Vsel**1** correspond to the compensation stage of threshold voltage Si and the lighting stage S**2** successively.

In another embodiment, a data signal Vdata**1** and a scanning signal Vsel**1** both are generated through an external timing controller. A first reference voltage signal Vref**1**, a second reference voltage signal Vref**2**, a power signal Vdd**1** all are generated through a constant voltage source.

The data signal Vdata**1** is a display data signal VDATA**1** at high voltage level, and the scanning signal Vsel**1** is at high voltage level during the compensation stage of threshold voltage S**1** so that the first TFT T**1**, the second TFT T**2**, the third TFT T**3**, and the fourth TFT T**4** all are turned on. The data signal Vdata**1** writes the display data signal VDATA**1** at high voltage level into the source of the first TFT T**1** through the third TFT T**3** and the fourth TFT T**4**. The first reference voltage Va provided by the first reference voltage signal Vref**1** is written into the gate of the first TFT T**1** through the second TFT T**2**.

That is, during the compensation stage of threshold voltage S**1**, equations are as follows:

$$V_g = V_a; \tag{1}$$

$$V_s = V_a - \left[\left(\frac{W}{L}\right)_{T4} \Big/ \left(\frac{W}{L}\right)_{T1}\right]^{\frac{1}{2}} (VDATA1 - Vb - Vth3) - Vth1;$$

$$V_{gs} = V_g - V_S = \left[\left(\frac{W}{L}\right)_{T4} \Big/ \left(\frac{W}{L}\right)_{T1}\right]^{\frac{1}{2}} (VDATA1 - Vb - Vth3) + Vth1.$$

where Vg indicates the voltage level of the first node g (i.e., the voltage level of the gate of the first TFT T**1**); Vs indicates the voltage level of the second node s (i.e., the voltage level of the source of the first TFT T**1**); Vgs indicates the voltage across a gate and a source of the first TFT T**1**; Va indicates a first reference voltage, and Vb indicates a second reference voltage;

$$\left(\frac{W}{L}\right)_{T4}$$

indicates the ratio of the width to the length of a channel of the fourth TFT T**4**;

$$\left(\frac{W}{L}\right)_{T1}$$

indicates the ratio of the width to the length of a channel of the first TFT T**1**; VDATA**1** is a data signal at high voltage level; Vth**3** is a threshold voltage imposed on the third TFT T**3**; Vth**1** is the threshold voltage imposed on the first TFT T**1**.

The data signal Vdata**1** is at low voltage level, and the scanning signal Vsel**1** is at low voltage level during the lighting stage S**2** so that the first TFT T**1** and the fourth TFT T**4** are turned on, and the second TFT T**2** and the third TFT T**3** are disconnected. The gate-source voltage V_{gs} imposed on the first TFT T**1** remains stable under the function of storage of the capacitor C**1**.

The gate-source voltage V_{gs} for driving the OLED D**1** to light includes a threshold voltage imposed on the first TFT T**10**. The electric current flowing through the OLED D**1** and the square of the difference of the gate-source voltage V_{gs} and the threshold voltage imposed on the first TFT T**10** are in direct proportion. Therefore, the electric current flowing through the OLED D**1** is irrelevant to the threshold voltage imposed on the first TFT T**10**, that is, the driving TFT. In other words, the threshold voltage is compensated.

At the compensation stage of threshold voltage Si in the present embodiment, the gate of the fourth TFT T**4** is controlled by the data signal at high voltage level VDATA**1**, and the source is controlled by the second reference voltage Vb so the electric current flowing through the first TFT T**10** is well controlled by the data signal at high voltage level VDATA**1** and the second reference voltage Vb. At the lighting stage S**2**, the third TFT T**3** can prevent the second reference voltage Vb from affecting the voltage level of the gate of the first TFT T**10**.

In the present embodiment, to ensure the first TFT T**1** is turned on normally in the working process of the pixel driving circuit **100**, the second reference voltage Vb needs to satisfy the following equation:

$$Vb < VDATA1 - Vth3^{\circ} \tag{2}$$

In the present embodiment, to ensure the first TFT T**1** is turned on normally during the compensation stage of threshold voltage S**1**, the first TFT T**1** is turned on normally while the OLED D**1** cannot be turned on. The first reference voltage Va satisfies the following equation:

$$\left[\left(\frac{W}{L}\right)_{T4} \Big/ \left(\frac{W}{L}\right)_{T1}\right]^{\frac{1}{2}} (VDATA1 - Vb - Vth3) - Vth1 + Voled1 > Va \tag{3}$$

and

$$Va > \left[\left(\frac{W}{L}\right)_{T4} \Big/ \left(\frac{W}{L}\right)_{T1}\right]^{\frac{1}{2}} (VDATA1 - Vb - Vth3) - Vth1.$$

where Voled**1** indicates voltage level of an anode node level of the OLED D**1** during the compensation stage of threshold voltage.

FIG. **5** is a circuit diagram of a pixel driving circuit **200** according to a second embodiment of the present disclosure. The difference between the pixel driving circuit **200** and the pixel driving circuit **100** as FIG. **3** illustrates is that a first reference voltage signal Vref**1** is a power signal Vdd**1** in the pixel driving circuit **200**.

That is, no first reference signals Vref**1** are in the pixel driving circuit **200**. A source of the second TFT T**2** is directly connected to the power signal Vdd**1**.

Please refer to FIG. **6** as well. FIG. **6** illustrates a timing diagram of a pixel driving circuit **200** as illustrated in FIG. **5**. The difference between the pixel driving circuit **200** and the pixel driving circuit **100** as FIG. **4** illustrates is the working process. In the pixel driving circuit **200** as FIG. **6** illustrates, the power signal Vdd**1** is at referring low voltage level during the compensation stage of threshold voltage S**1**.

The referring low voltage level is a first reference voltage Va. The power signal Vdd**1** is at high voltage level during the lighting stage S**2**.

The power signal Vdd**1**, the data signal Vdata**1**, and the scanning signal Vsel**1** all are generated through an external timing controller in the present embodiment. A second reference voltage signal Vref**2** is generated through a constant voltage source.

In the present embodiment, the voltage level of a gate of the first TFT T**1**, the voltage level of the source of the first TFT T**1**, and the gate-source voltage V_{gs} satisfy the equation (1). The first reference voltage Va satisfies the equation (3). The second reference voltage Vb satisfies the equation (2).

Different from the first embodiment, the first reference voltage Va is the referring low voltage level of the power signal Vdd**1** in the present embodiment.

Please refer to FIG. **7** and FIG. **8**. FIG. **7** illustrates a relationship of the electric current I_{OLED} flowing through the OLED when a drift value ΔVth of the threshold voltage Vth of the conventional 2T1C driving TFT (i.e., the first TFT T**10**) and a drift value ΔVoled of the threshold voltage Vth**1** of the first TFT T**1** are 0 volts, +0.5V, and −0.5V. FIG. **8** illustrates a relationship of the electric current I_{OLED} flowing through the OLED when a drift value ΔVth of the threshold voltage Vth of the driving TFT (i.e., the first TFT T**10**) **100** or **200** in the present disclosure and a drift value ΔVoled of the threshold voltage Vth**1** of the first TFT T**1** are 0 volts, +0.5V, and −0.5V. Compared FIG. **7** and FIG. **8**, the variation of the electric current flowing through the OLED in the present disclosure is obviously less than the variation of the electric current flowing through the OLED in the 2T1C driving TFT without any compensation. Therefore, the threshold voltage of the driving TFT can be effectively compensated. Not only lighting stability of the OLED is ensured but also the display brightness of the OLED display panel keeps stable. The threshold voltage does not vary with use time, which means that the display quality is improved.

FIG. **9** is a schematic diagram of an organic light-emitting diode (OLED) display **1** according to an embodiment of the present disclosure. The OLED display **1** includes a pixel driving circuit **2**. The pixel driving circuit **2** is the pixel driving circuit **100** or the pixel driving circuit **200**.

The present disclosure can bring beneficiary effects as describes: The fourth TFT is introduced in the pixel driving circuit and the OLED display device to control the electric current of the first TFT with the data signal and the second reference signal during the compensation stage of threshold voltage. Further, the compensation voltage of the first TFT (i.e., a driving TFT) is compensated. Because of the introduction of the third TFT, the voltage level of a gate of the first TFT prevents from being affected by the second reference voltage sign during the lighting stage.

The present disclosure is described in detail in accordance with the above contents with the specific preferred examples. However, this present disclosure is not limited to the specific examples. For the ordinary technical personnel of the technical field of the present disclosure, on the premise of keeping the conception of the present disclosure, the technical personnel can also make simple deductions or replacements, and all of which should be considered to belong to the protection scope of the present disclosure.

What is claimed is:

1. A pixel driving circuit, comprising: a first thin-film transistor (TFT), a second TFT, a third TFT, a fourth TFT, a capacitor, and an organic light-emitting diode (OLED);

a gate of the first TFT electrically connected to a first node, a source of the first TFT electrically connected to a second node, a drain of the first TFT electrically connected to a power signal;

a gate of the second TFT electrically connected to a scanning signal, a source of the second TFT electrically connected to a first reference voltage signal, a drain of the second TFT electrically connected to the first node;

a gate of the third TFT electrically connected to the scanning signal; a source of the third TFT electrically connected to a drain of the fourth TFT; a drain of the third TFT is electrically connected to the second node;

a gate of the fourth TFT electrically connected to a data signal, a source of the fourth electrically connected to a second reference voltage signal;

one terminal of the capacitor electrically connected to the first node; the other terminal of the capacitor electrically connected to the second node;

an anode of the OLED electrically connected to the second node; a cathode of the OLED electrically connected to a ground terminal;

wherein the first reference voltage signal is the power signal,

wherein a voltage across a gate and a source of the first TFT satisfies the following equation:

$$V_{gs} = \left[\left(\frac{W}{L}\right)_{T4} \Big/ \left(\frac{W}{L}\right)_{T1}\right]^{\frac{1}{2}} (VDATA1 - Vb - Vth3) + Vth1;$$

where Vgs indicates the voltage across a gate and a source of the first TFT; Vb indicates a second reference voltage provided by the second reference voltage signal;

$$\left(\frac{W}{L}\right)_{T4}$$

indicates the ratio of the width to the length of a channel of the fourth TFT;

$$\left(\frac{W}{L}\right)_{T1}$$

indicates the ratio of the width to the length of a channel of the first TFT; VDATA**1** is a display data signal at high voltage level provided by the data signal; Vth**3** is a threshold voltage imposed on the third TFT; Vth**1** is the threshold voltage imposed on the first TFT.

2. The pixel driving circuit of claim **1**, wherein the second reference voltage signal is constant low voltage; the power signal, the data signal, and the scanning signal correspond to a compensation stage of threshold voltage and a lighting stage;

during the compensation stage of threshold voltage, the power signal is at referring low voltage level: the data signal is the display data signal at high voltage level; the scanning signal is at high voltage level;

during the lighting stage, the power signal is at high voltage level; the data signal is at low voltage level; the scanning signal is at low voltage level.

3. A pixel driving circuit, comprising: a first thin-film transistor (TFT), a second TFT, a third TFT, a fourth TFT, a capacitor, and an organic light-emitting diode (OLED);

a gate of the first TFT electrically connected to a first node, a source of the first TFT electrically connected to a second node, a drain of the first TFT electrically connected to a power signal;

a gate of the second TFT electrically connected to a scanning signal, a source of the second TFT electrically connected to a first reference voltage signal, a drain of the second TFT electrically connected to the first node;

a gate of the third TFT electrically connected to the scanning signal; a source of the third TFT electrically connected to a drain of the fourth TFT; a drain of the third TFT is electrically connected to the second node;

a gate of the fourth TFT electrically connected to a data signal, a source of the fourth electrically connected to a second reference voltage signal;

one terminal of the capacitor electrically connected to the first node; the other terminal of the capacitor electrically connected to the second node;

an anode of the OLED electrically connected to the second node; a cathode of the OLED electrically connected to a ground terminal.

4. The pixel driving circuit of claim **3**, wherein the first reference voltage signal is the power signal.

5. The pixel driving circuit of claim **4**, wherein the second reference voltage signal is constant low voltage; the power signal, the data signal, and the scanning signal correspond to a compensation stage of threshold voltage and a lighting stage;

during the compensation stage of threshold voltage, the power signal is at referring low voltage level; the data signal is the display data signal at high voltage level; the scanning signal is at high voltage level;

during the lighting stage, the power signal is at high voltage level; the data signal is at low voltage level; the scanning signal is at low voltage level.

6. The pixel driving circuit of claim **5**, wherein the power signal, the data signal, and the scanning signal all are generated through an external timing controller.

7. The pixel driving circuit of claim **3**, wherein the first reference voltage signal and the second reference voltage signal both are constant low voltage; the power signal is constant high voltage; the data signal and the scanning signal correspond to a compensation stage of threshold voltage and a lighting stage successively;

the data signal is a display data signal at high voltage level, and the scanning signal Vsel **1** is at high voltage level during the compensation stage of threshold voltage;

the data signal is at low voltage level; the scanning signal is at low voltage level during the lighting stage.

8. The pixel driving circuit of claim **7**, wherein the data signal and the scanning signal both are generated through an external timing controller.

9. The pixel driving circuit of claim **3**, wherein a voltage across a gate and a source of the first TFT satisfies the following equation:

$$V_{gs} = \left[\left(\frac{W}{L}\right)_{T4} \Big/ \left(\frac{W}{L}\right)_{T1}\right]^{\frac{1}{2}} (VDATA1 - Vb - Vth3) + Vth1;$$

where Vgs indicates the voltage across a gate and a source of the first TFT; Vb indicates a second reference voltage provided by the second reference voltage signal;

$$\left(\frac{W}{L}\right)_{T4}$$

indicates the ratio of the width to the length of a channel of the fourth TFT;

$$\left(\frac{W}{L}\right)_{T1}$$

indicates the ratio of the width to the length of a channel of the first TFT; VDATA**1** is a display data signal at high voltage level provided by the data signal; Vth**3** is a threshold voltage imposed on the third TFT; Vth**1** is the threshold voltage imposed on the first TFT.

10. The pixel driving circuit of claim **3**, wherein the second reference voltage Vb provided by the second reference signal needs to satisfy the following equation:

$$Vb < VDATA1 - Vth3;$$

where a display data signal at high voltage level provided by the data signal is a threshold voltage of the third TFT.

11. The pixel driving circuit of claim **3**, wherein the TFT, the second TFT, the third TFT, and the fourth TFT all are low temperature poly-silicon (LTPS) TFTs, oxide semiconductor TFTs, or amorphous silicon (α-Si) TFTs.

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专利名称(译)	像素驱动电路和OLED显示装置有效地补偿施加在驱动TFT上的阈值电压		
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摘要(译)

提供像素驱动电路和OLED显示器。像素驱动电路包括第一TFT，第二TFT，第三TFT，第四TFT，电容器和OLED。第三TFT的栅极耦合到扫描信号。第三TFT的源极耦合到第四TFT的漏极。第四TFT的栅极耦合到数据信号，第四TFT的源极耦合到第二参考电压信号。第四TFT在阈值电压的补偿阶段期间利用数据信号和第二参考信号控制第一TFT的电流。此外，补偿第一TFT的补偿电压。